Attorney's Docket No.: 10559-535001/P12545

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: John A. Wishneusky	Art Unit:	2182
Serial No.:	09/989,483	Examiner:	
Filed	: November 19, 2001		
Assignee	: Intel Corporation		
Title	: CONTEXT EXECUTION IN A PIPELINED COMPUTER PROCESSOR		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicants call attention to the attached Information Disclosure Statement and documents listed on form PTO-1449.

This filing is being made before the receipt of a first Office action on the merits. No fee is required.

Each enclosed document listed on the herewith Form PTO-1449 was cited in the attached International Search Report dated November 27, 2003, issued in a foreign counterpart application not more than three months ago. To the best knowledge of the undersigned, this is the first citation of these items in any

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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communication from a foreign patent office in a counterpart

foreign application.

The documents are in the English language; hence no concise

explanation is necessary per Rule 98(a)(3).

Consideration of the foregoing and enclosures plus the

return of a copy of the enclosed form PTO-1449 with the

Examiner's initials in the left column per MPEP 609 are

earnestly solicited along with an early action on the merits.

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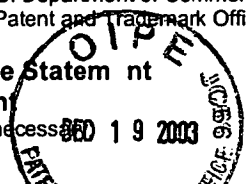
Account No. 06-1050.

Respectfully submitted,

Date: 8/17/03

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Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-535001	Application No. 09/989,483

Information Disclosure Statement by Applicant
(Use several sheets if necessary)
(37 CFR §1.98(b))

Applicant	
John A. Wishneusky	
Filing Date November 19, 2001	Group Art Unit 2182

[Stamp: OIPE DEC 1 9 2003 PATENT & TRADEMARK OFFICE]

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

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Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	AL							
	AM							
	AN							
	AO							
	AP							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	AQ	Li, Yamin, et al., "The Effects of STEF in Finely Parallel Multithread Processors", *IEEE International Symposium on High-Performance Computer Architecture*, pp. 318-325, January 1995.
	AR	Loikkanen, et al., "A Fine-Grain Multithreading Superscalar Architecture", *IEEE Comp. Soc.*, pp.163-168, October 1996.
	AS	Thistle, et al., "A Processor Architecture for Horizon", *IEEE Proceedings Supercomputing*, pp. 35-41, November 1988.
	AT	

Examiner Signature	Date Considered

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Disclosure Form (PTO-1449)